IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) [[A]] In a computer-aided design and verification system, a method for ~~overriding a~~ facilitating signal override ~~during model simulation~~ in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said method comprising:

~~instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal;~~

~~declaring a signal override during model simulation; and~~

~~in response to said declared signal override, selecting said override signal utilizing said signal selection means~~

instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including:

an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and

an output port mapping field comprising an override signal field specifying the name of said override signal, a port name field specifying the name of the port from which said override signal is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden.

2. (Currently Amended) The method of claim [[1]] 13, wherein said ~~declaring step~~ output port mapping field further comprises ~~instantiating an override enable port~~ a control port field specifying an output port for delivering an override enable signal to said signal selection means.

3. (Canceled)

4. (Currently Amended) The method of claim 2, further comprising:

instantiating a latch ~~that~~ within said simulation model, wherein said latch stores an override disable bit; and

combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that ~~controls~~ determines whether or not said signal selection means overrides said designated signal with said override signal.

5. (Currently Amended) [[A]] In a computer-aided design and verification system, a system for ~~overriding a~~ facilitating signal override ~~during model simulation~~ in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said system comprising:

~~processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal;~~

~~processing means for declaring a signal override during model simulation; and~~

~~processing means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means~~

processing means for instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process, wherein said non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including:

an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and

an output port mapping field comprising an override signal field specifying the name of said override signal, a port name field specifying the name of the port from which said override signal is output from said instrumentation entity, and a target signal

field specifying the name of said designated signal to be overridden.

6. (Currently Amended) The system of claim [[5]] 14, wherein said ~~processing means for declaring a signal override~~ output port mapping field further comprises ~~processing means for instantiating an override enable port~~ a control port specifying an output port for delivering an override enable signal to said signal selection means.

7. (Canceled)

8. (Currently Amended) The system of claim 6, further comprising:

processing means for instantiating a latch ~~that~~ within said simulation model, wherein said latch stores an override disable bit; and

processing means for combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that ~~controls~~ determines whether or not said signal selection means overrides said designated signal with said override signal.

9. (Currently Amended) [[A]] In a computer-aided design and verification system, a computer program product for ~~overriding a~~ facilitating signal override ~~during model simulation~~ in a simulation model of a digital circuit design that includes one or more design entities described utilizing a hardware description language (HDL), said computer program product including computer-executable instructions for performing a method comprising:

~~processing means for instantiating an override signal port for delivering an override signal from an instrumentation entity to a signal selection means, wherein said signal selection means selects between said signal and said override signal;~~

~~instruction means for declaring a signal override during model simulation; and~~

~~instruction means responsive to said declared signal override, for selecting said override signal utilizing said signal selection means~~

instantiating an instrumentation entity within at least one of said one or more design entities using port mapping fields designated by a non-conventional HDL comment syntax, said non-conventional HDL comment syntax processed by a post-compiler instrumentation load tool to instantiate said instrumentation entity during a post-compile model build process, wherein said

non-conventional HDL comment syntax is recognized by an HDL compiler such that the HDL compiler does not instantiate said instrumentation entity into the digital circuit design, said port mapping fields further including:

an input port mapping field containing data representing an input port at which said instrumentation entity receives a designated signal to be overridden; and

an output port mapping field comprising an override signal field specifying the name of said override signal, a port name field specifying the name of the port from which said override signal is output from said instrumentation entity, and a target signal field specifying the name of said designated signal to be overridden.

10. (Currently Amended) The computer program product of claim [[9]] 15, wherein said ~~instruction means for declaring a signal override~~ output port mapping field further comprises ~~instruction means for instantiating an override enable port~~ a control port field specifying an output port for delivering an override enable signal to said signal selection means.

11. (Canceled)

12. (Currently Amended) The computer program product of claim 10, wherein said method further ~~comprising~~ comprises:

~~instruction means for~~ instantiating a latch ~~that~~ within said simulation model, wherein said latch stores an override disable bit; and

~~instruction means for~~ combining said override disable bit with said override enable signal within a logic gate to produce a combined selection signal that ~~controls~~ determines whether or not said signal selection means overrides said designated signal with said override signal.

13. (New) The method of claim 1, further comprising generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler instrumentation load tool processing said port mapping fields.

14. (New) The system of claim 5, further comprising processing means for generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler instrumentation load tool processing said port mapping fields.

15. (New) The computer program product of claim 9, wherein said method further comprises generating signal selection means within said simulation model for selectively overriding said designated signal with said override signal responsive to said post-compiler instrumentation load tool processing said port mapping fields.